

006260" 88452960

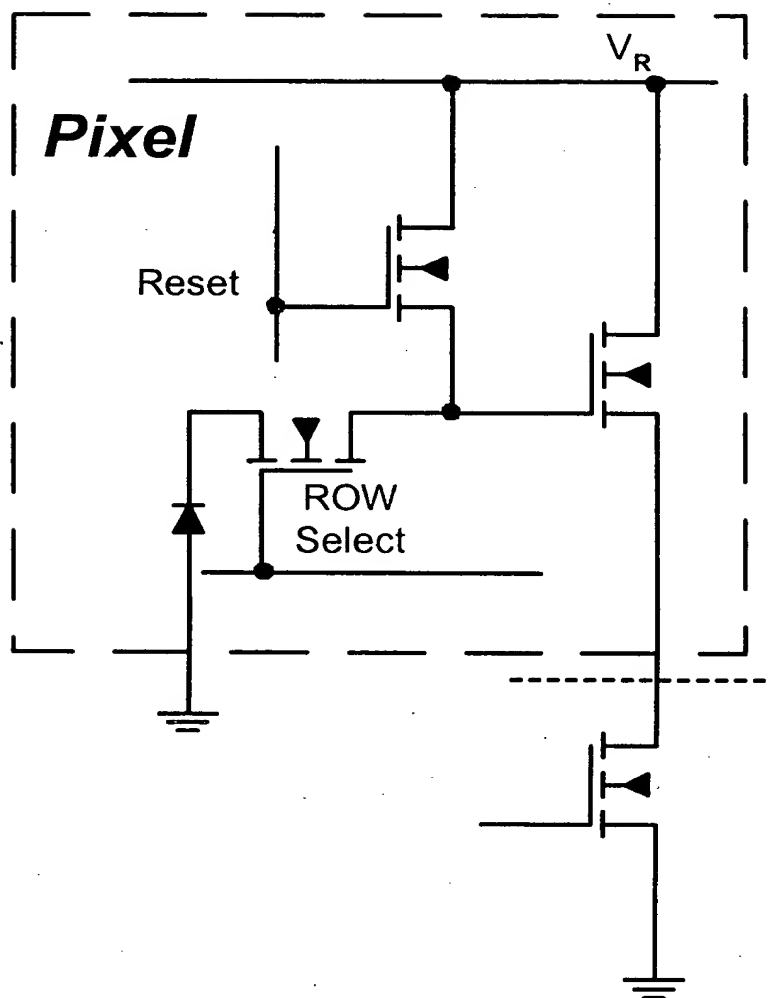


FIGURE 1 (PRIOR ART)

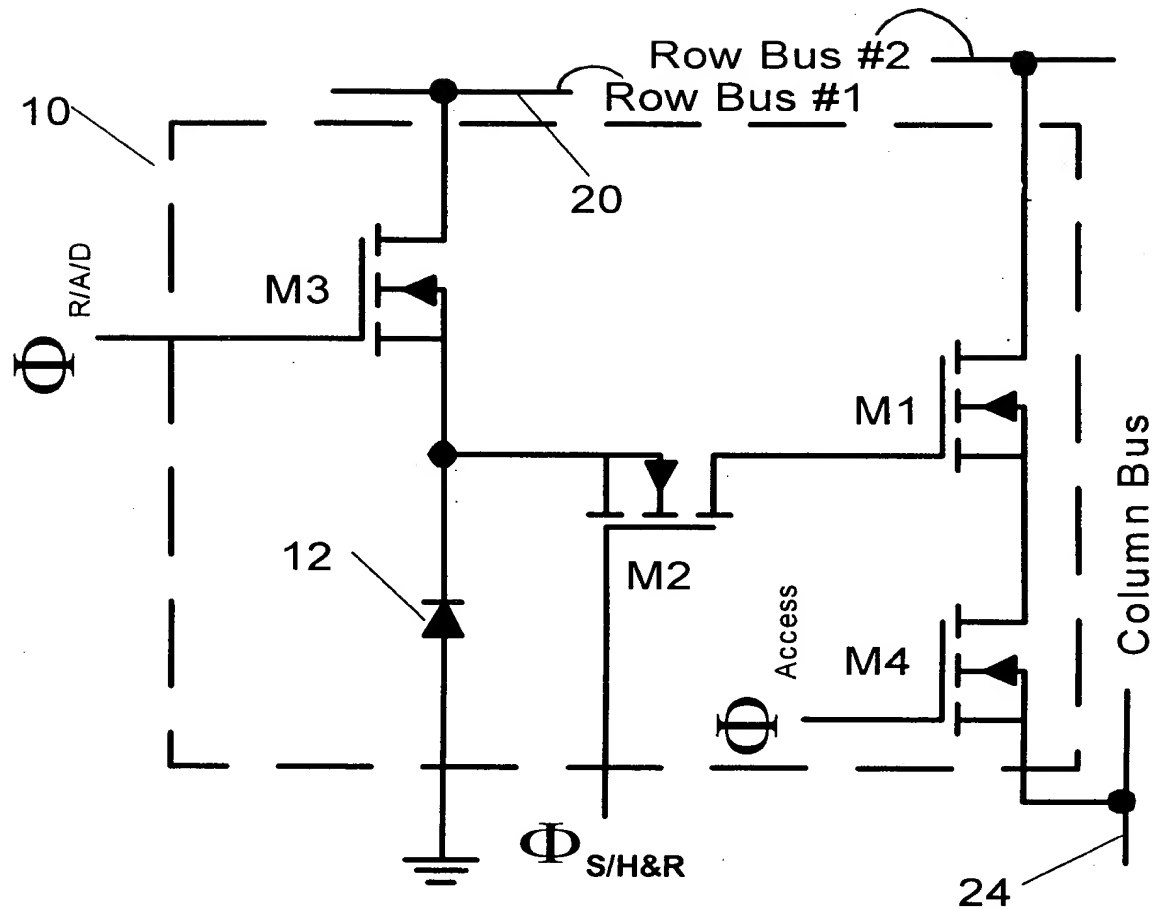


FIGURE 2

[illegible]

FIGURE 3 (RESET)

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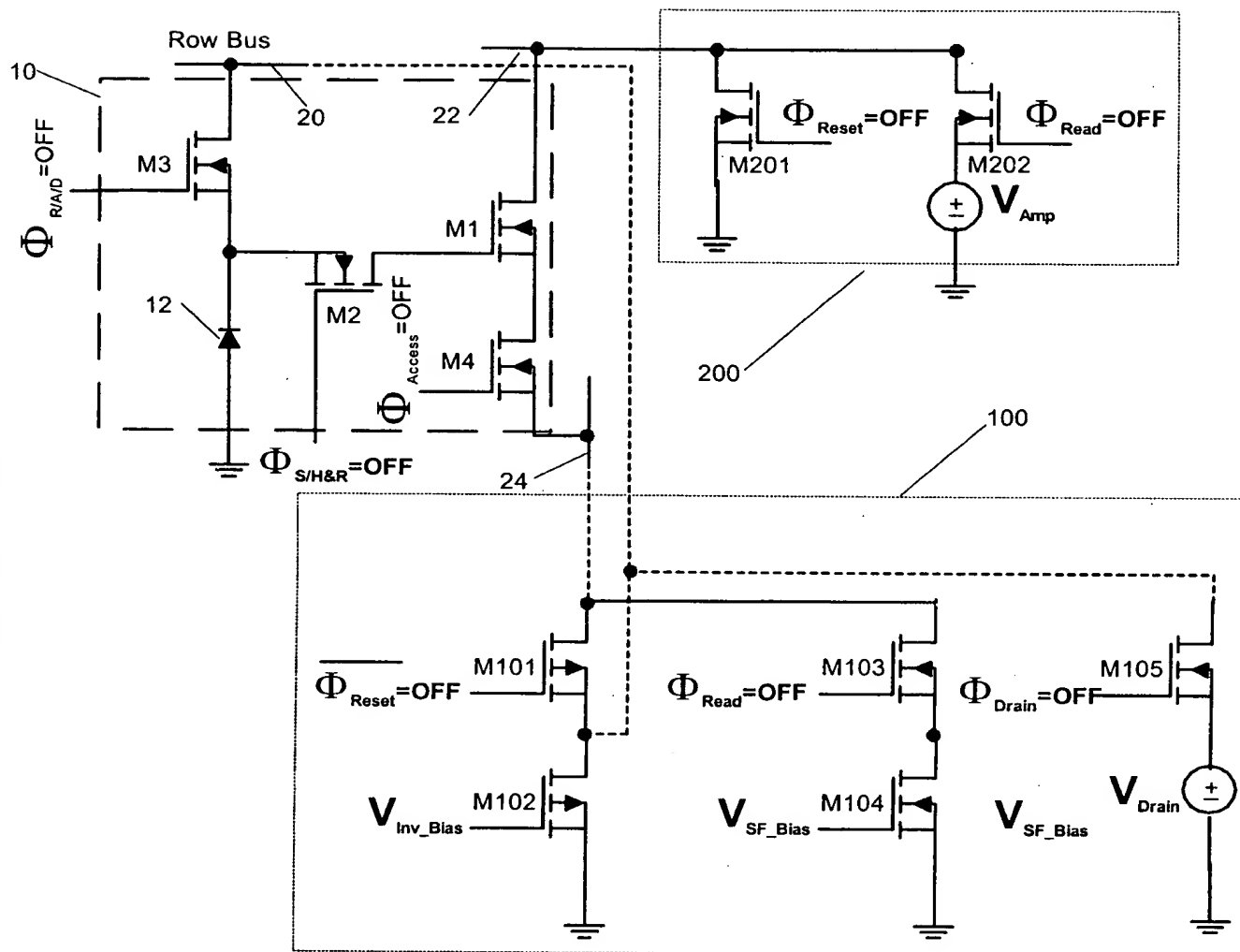


FIGURE 4 (INTEGRATE)

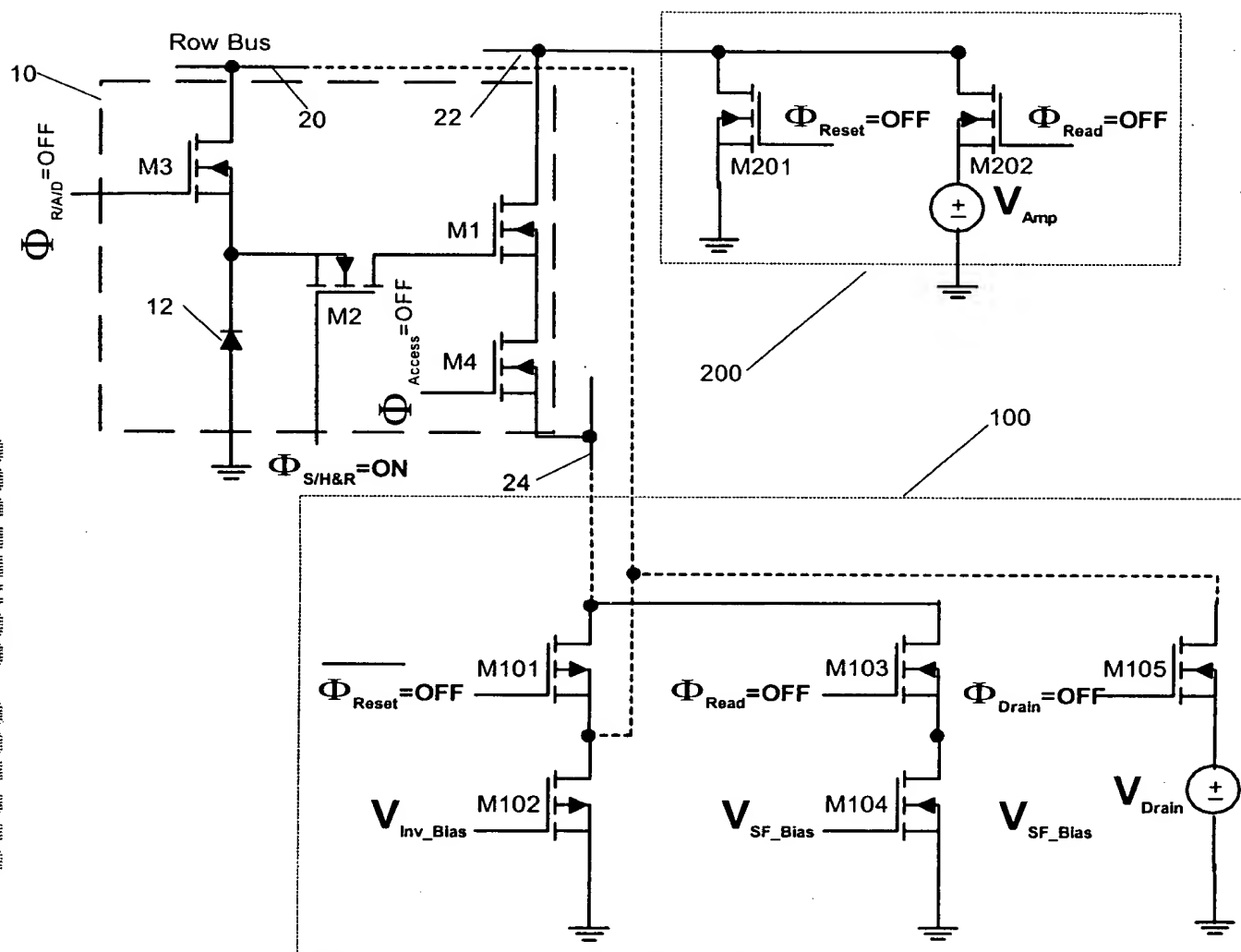
[illegible]

FIGURE 5 (SNAPSHOT)

The diagram illustrates a 1T1R1C1 SRAM cell and its associated read/write drivers. The SRAM cell (10) consists of a storage node (20) and an access node (22). The storage node is connected to a word line (24) and a bit line (12). The access node is connected to a word line (24) and a bit line (12). The storage node is also connected to a sense amplifier (200) and a read driver (100). The access node is connected to a sense amplifier (200) and a read driver (100). The sense amplifier (200) is a differential pair of transistors (M201, M202) with a current source (V_{Amp}). The read driver (100) is a differential pair of transistors (M101, M102) with a current source (V_{Inv_Bias}). The write driver (100) is a differential pair of transistors (M103, M104) with a current source (V_{SF_Bias}). The write driver (100) is also connected to a sense amplifier (200) and a read driver (100). The write driver (100) is also connected to a sense amplifier (200) and a read driver (100).

FIGURE 6 (READ)

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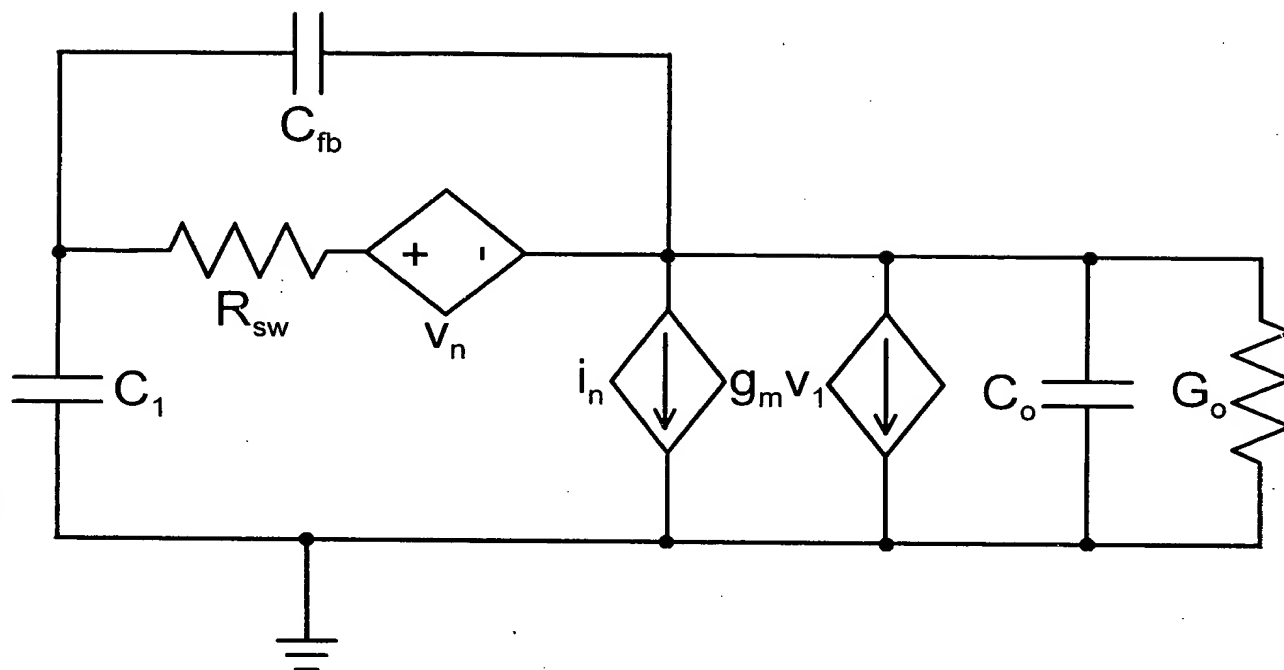


FIGURE 7

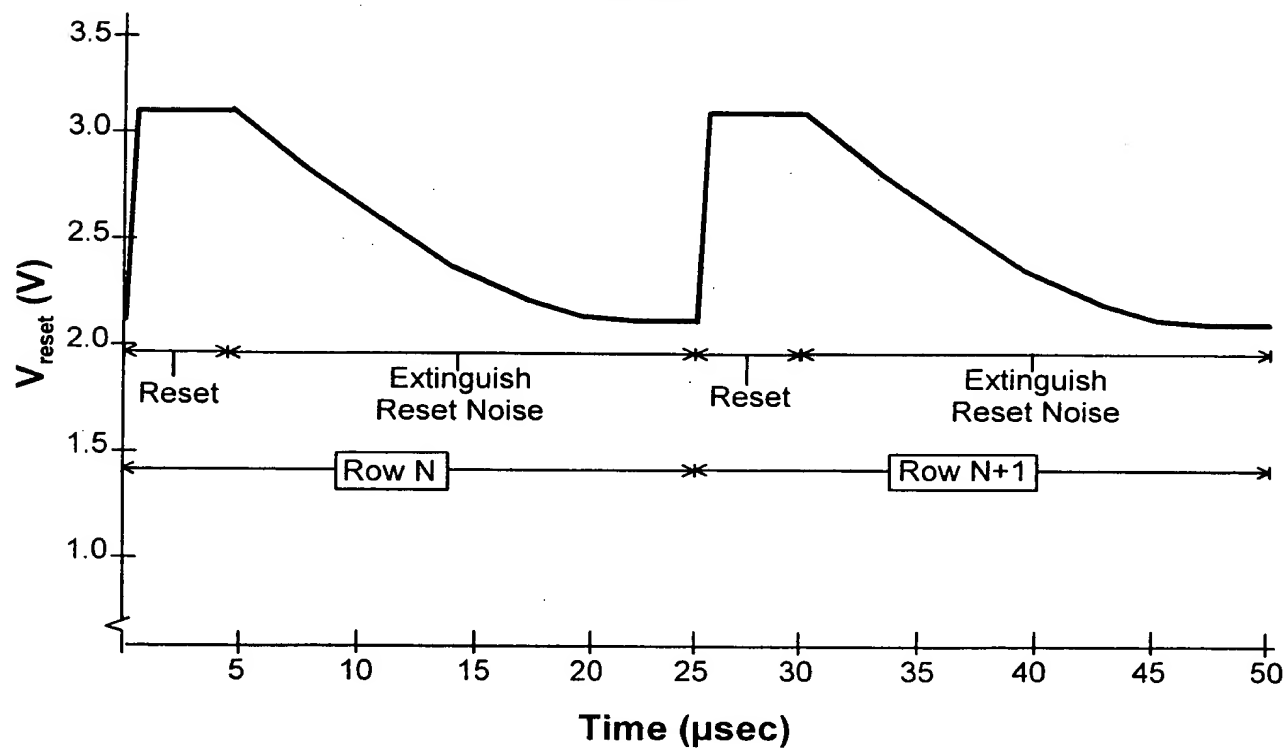


FIGURE 8